

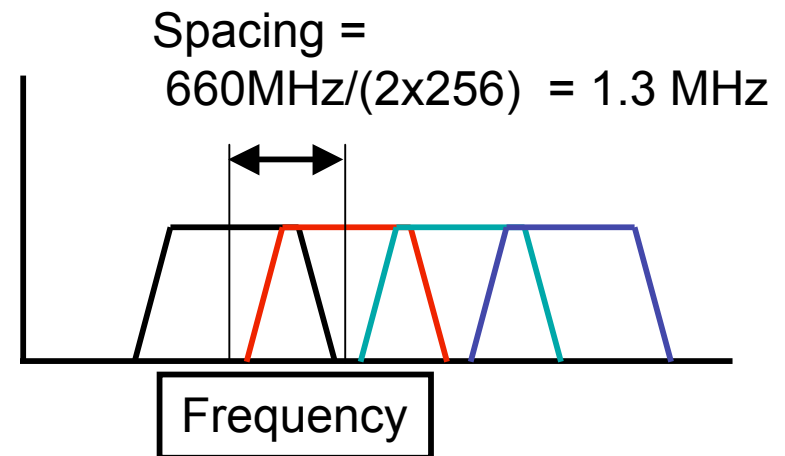
# Receiver Function:



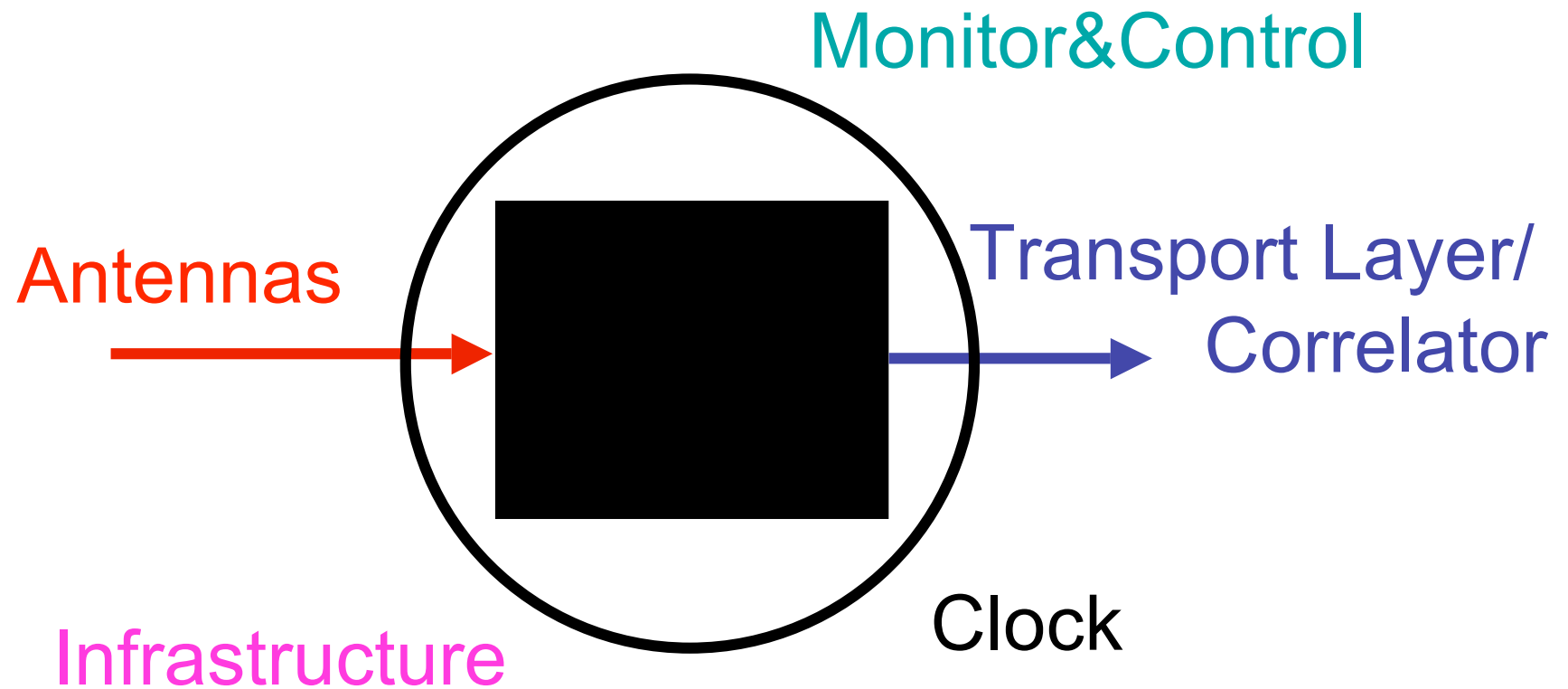
# Receiver Function:



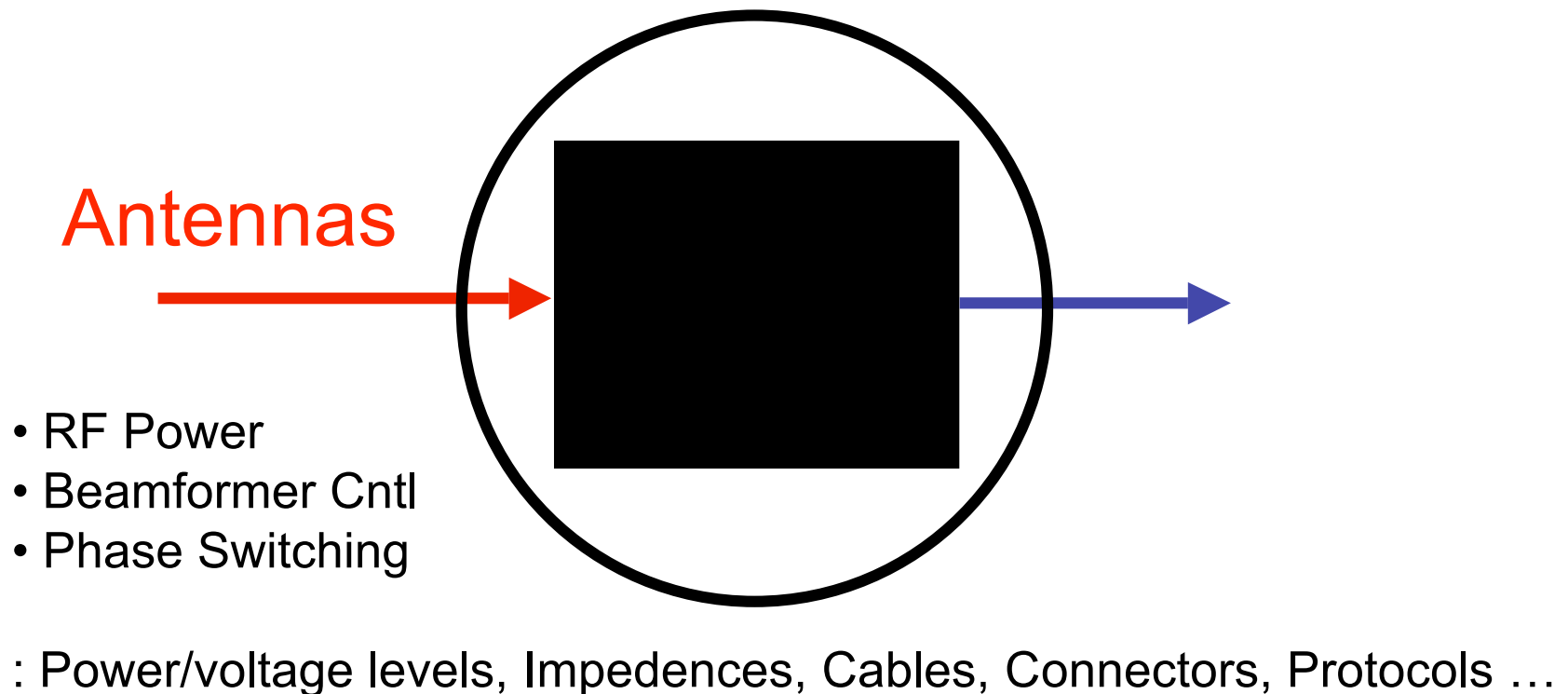
Channel Width =  
 $F_{\text{oversamp}} \times 660 \text{ MHz} / (2 \times 256) = 1.5 \text{ MHz}$



# Receiver Interfaces [WPs]:

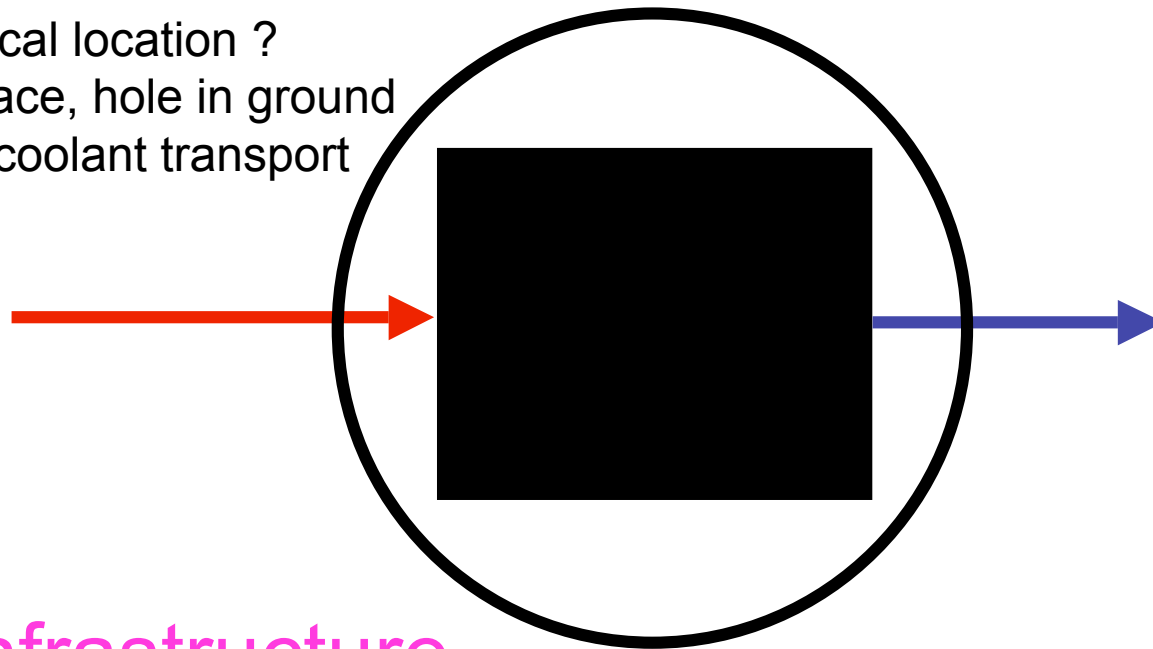


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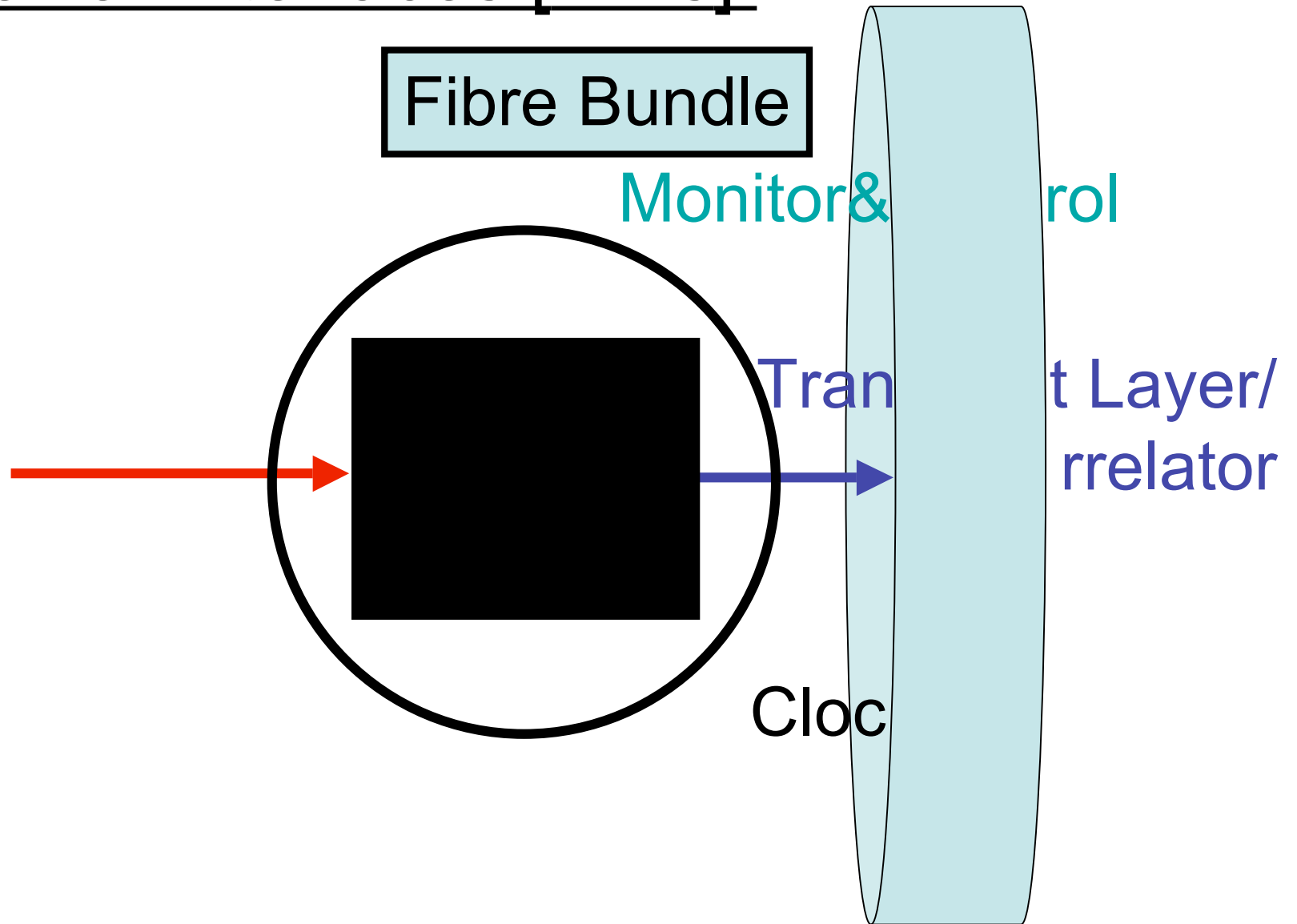
# Receiver Interfaces [WPs]:

- Power, voltages, ...
- comms, fibres, RF cables
- conduits
- physical location ?  
    surface, hole in ground
- heat/coolant transport



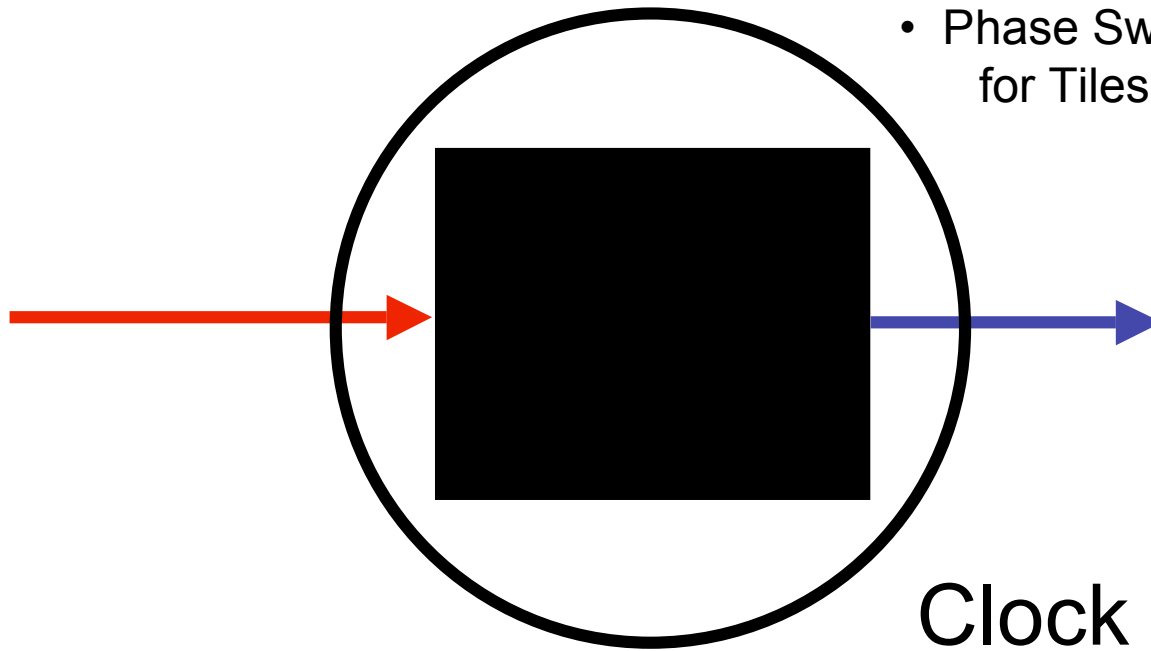
Infrastructure

# Receiver Interfaces [WPs]:

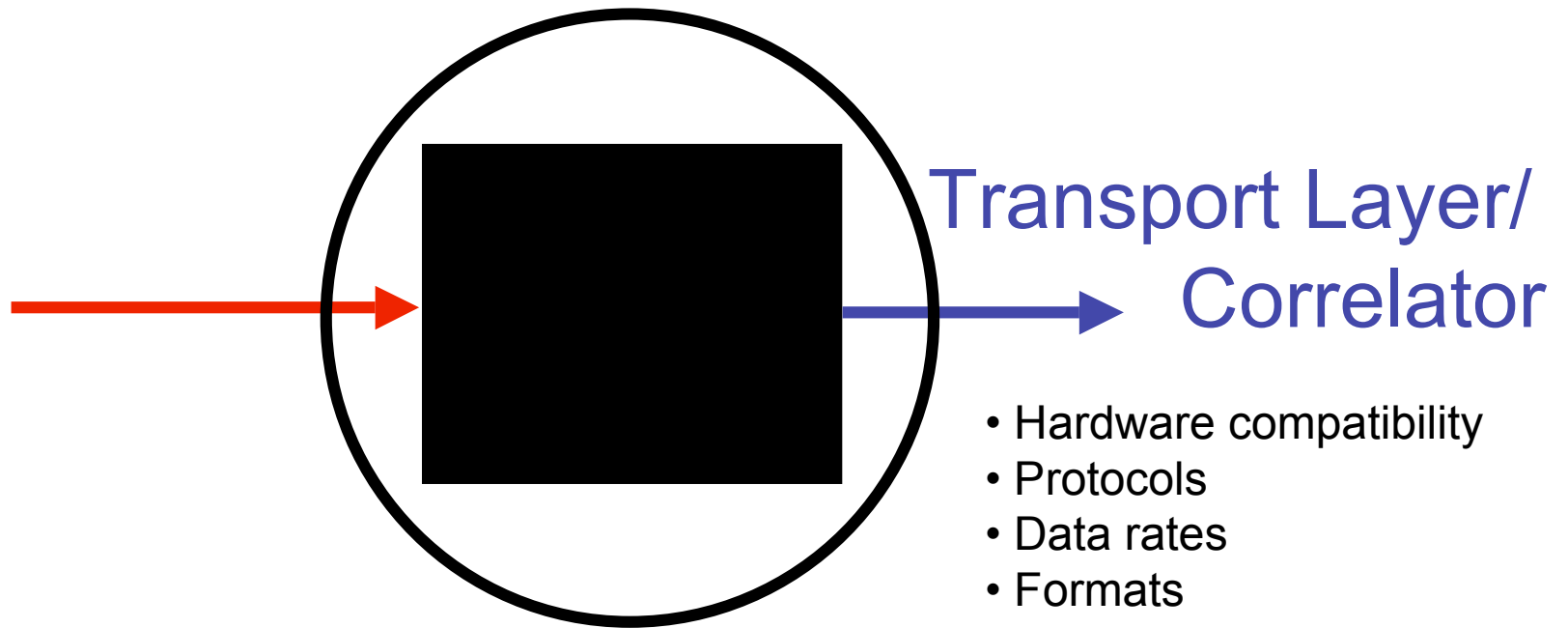


# Receiver Interfaces [WPs]:

- Clock “module” for Node
- Sampling Clock 660MHz (?)
- SCTN signal
- Phase Switching coordination for Tiles



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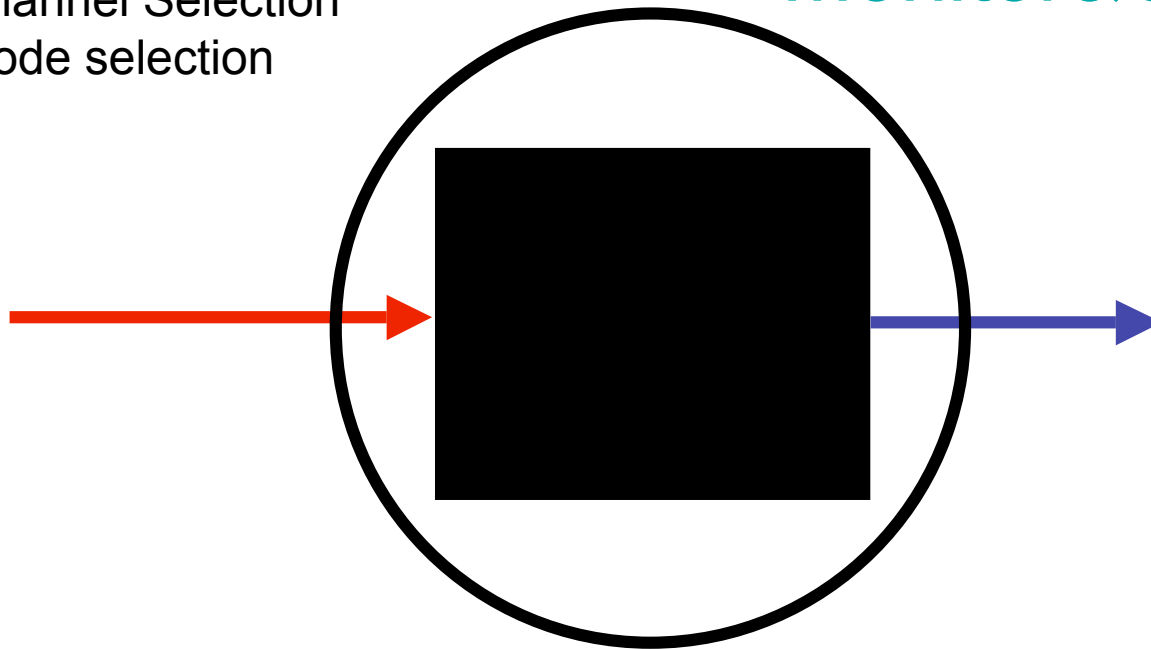


Distances...  $\leq$  array  
config & location of  
correlator, etc.

# Receiver Interfaces [WPs]:

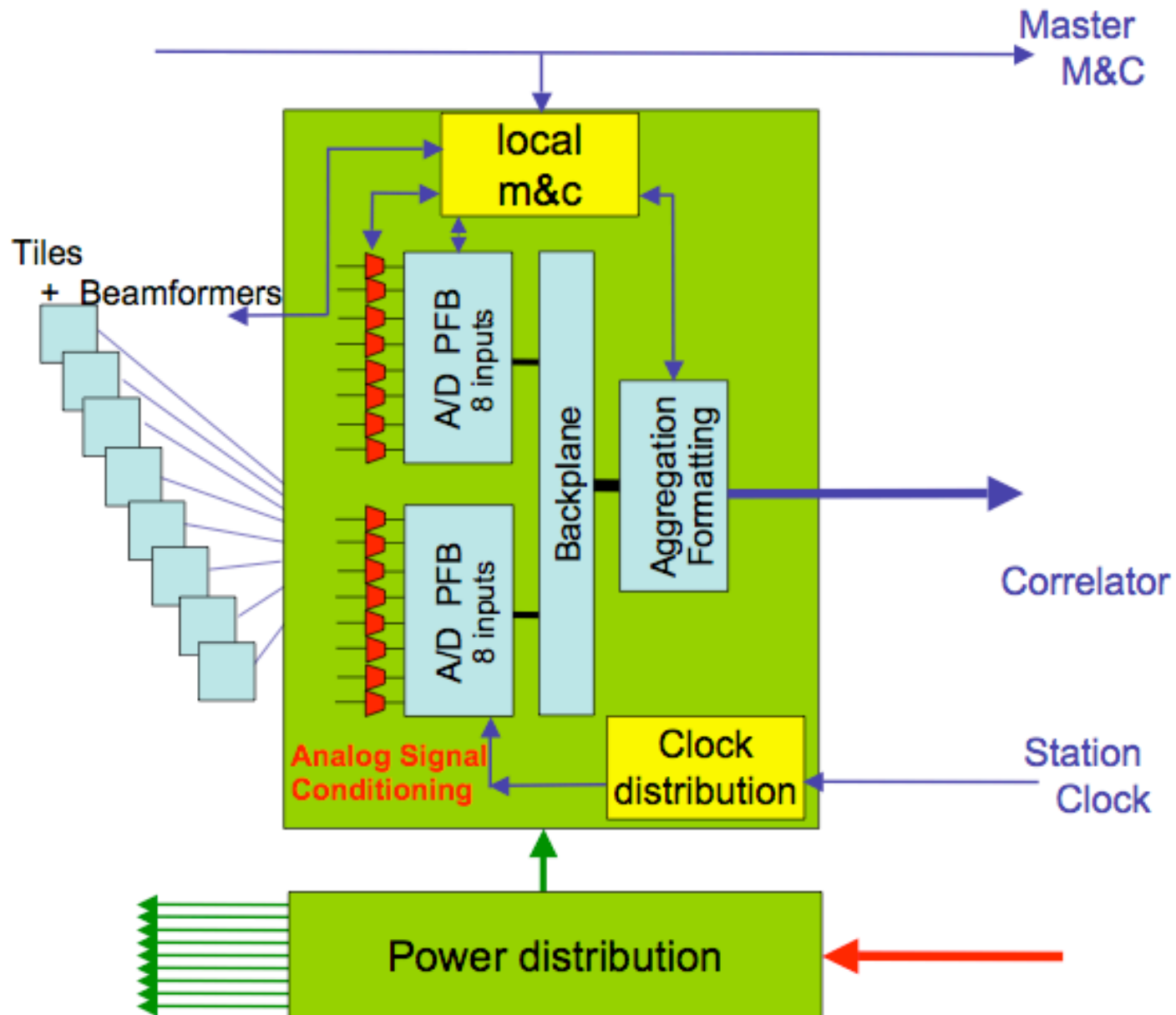
- to/from Tiles
- to/from Receiver
  - Gains
  - Channel Selection
  - Mode selection

Monitor&Control



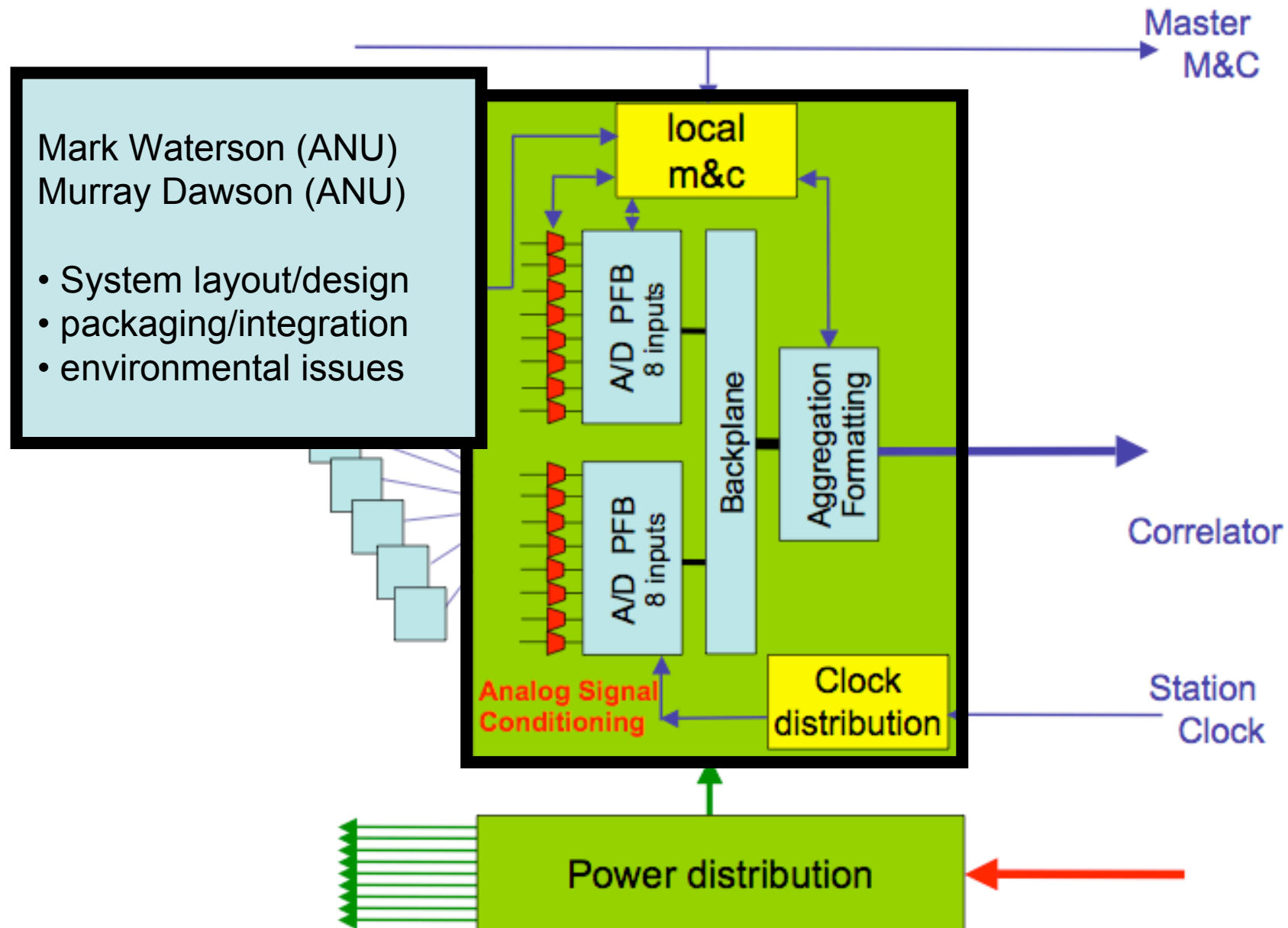
# 32T / Prototyping Layout !

## Receiver Node principal components



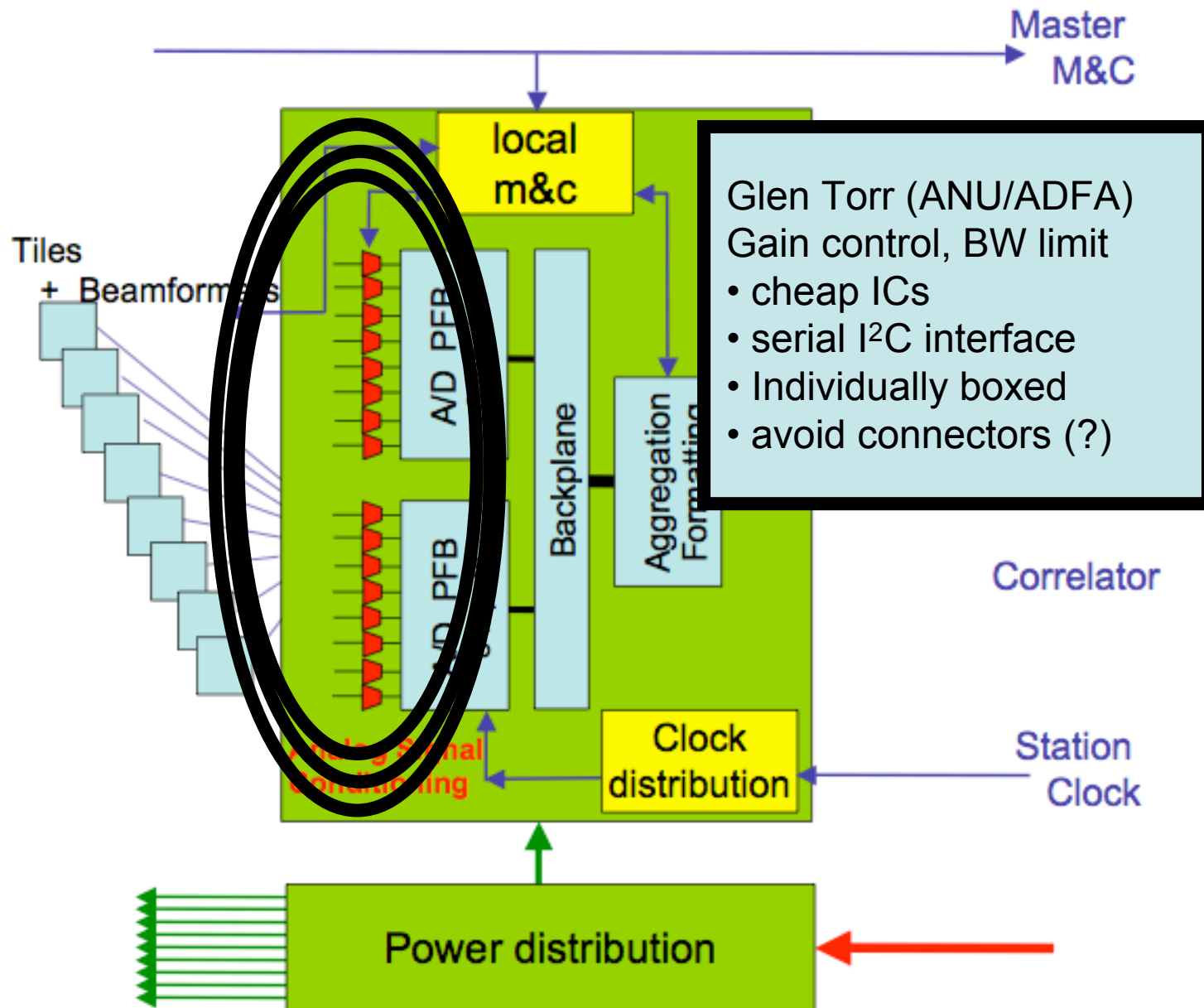
# 32T / Prototyping Layout !

## Receiver Node principal components



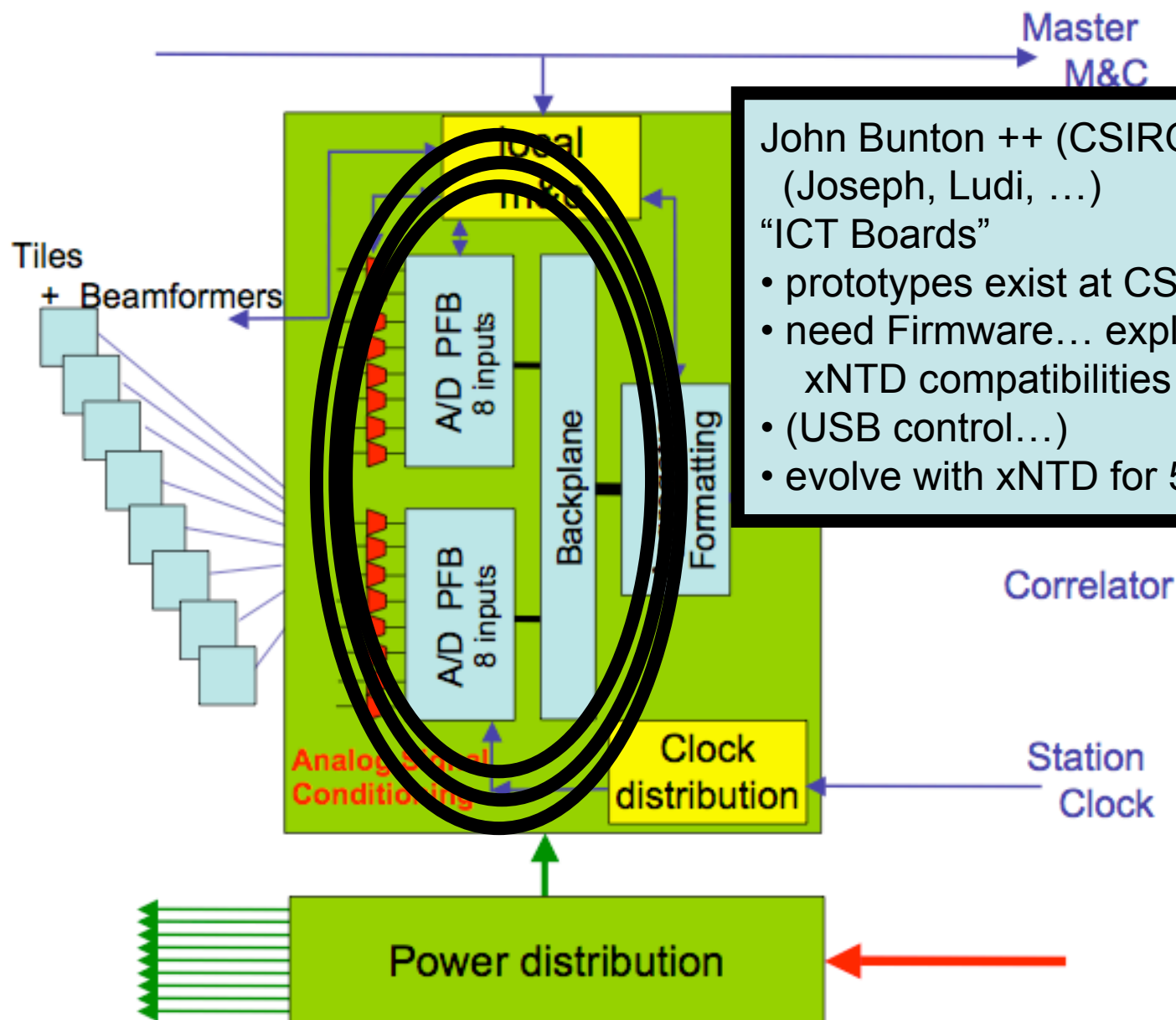
# 32T / Prototyping Layout !

## Receiver Node principal components



# 32T / Prototyping Layout !

## Receiver Node principal components



John Bunton ++ (CSIRO/ATNF)  
(Joseph, Ludi, ...)  
"ICT Boards"

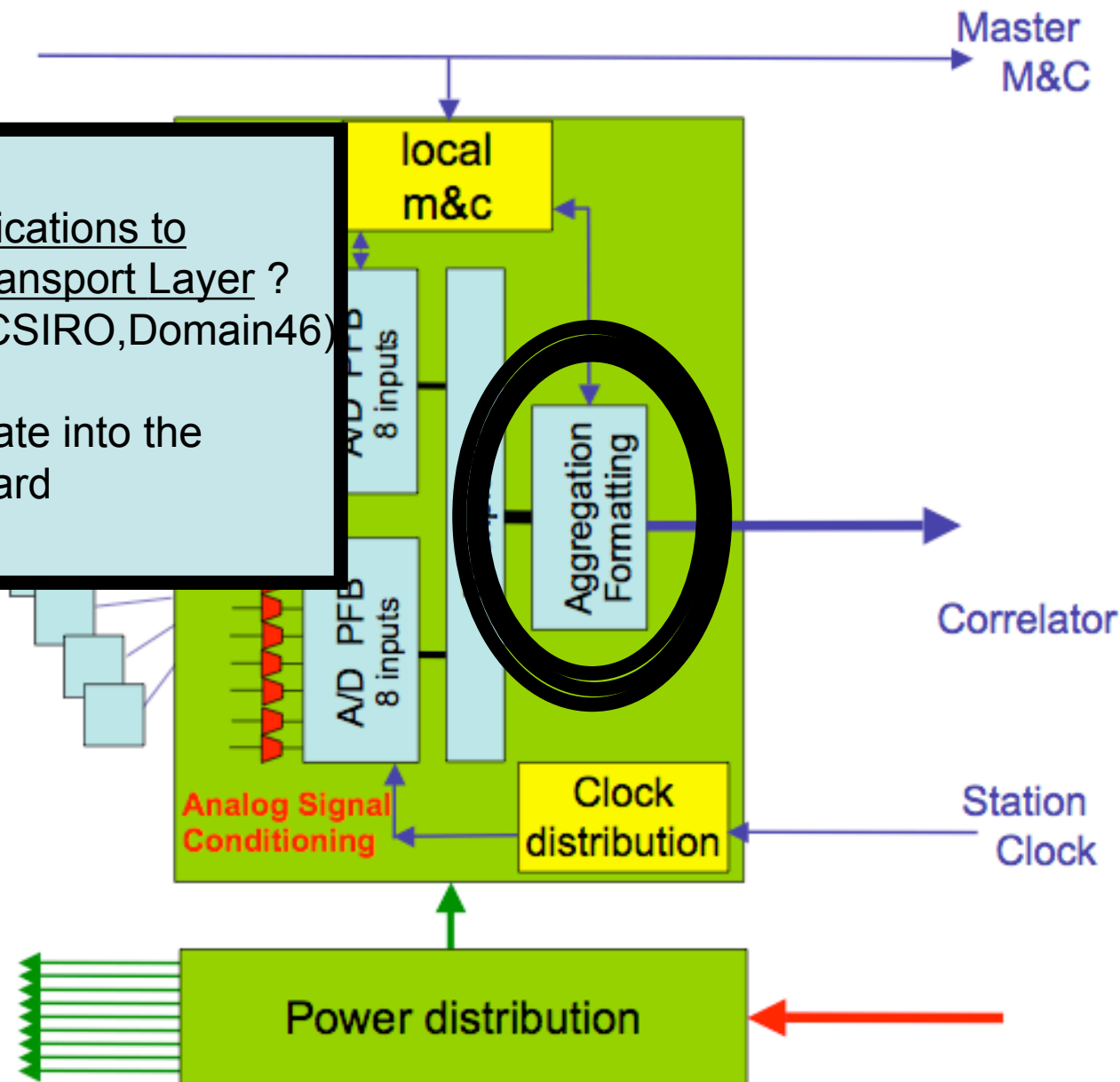
- prototypes exist at CSIRO
- need Firmware... exploit xNTD compatibilities
- (USB control...)
- evolve with xNTD for 500T ?

# 32T / Prototyping Layout !

## Receiver Node principal components

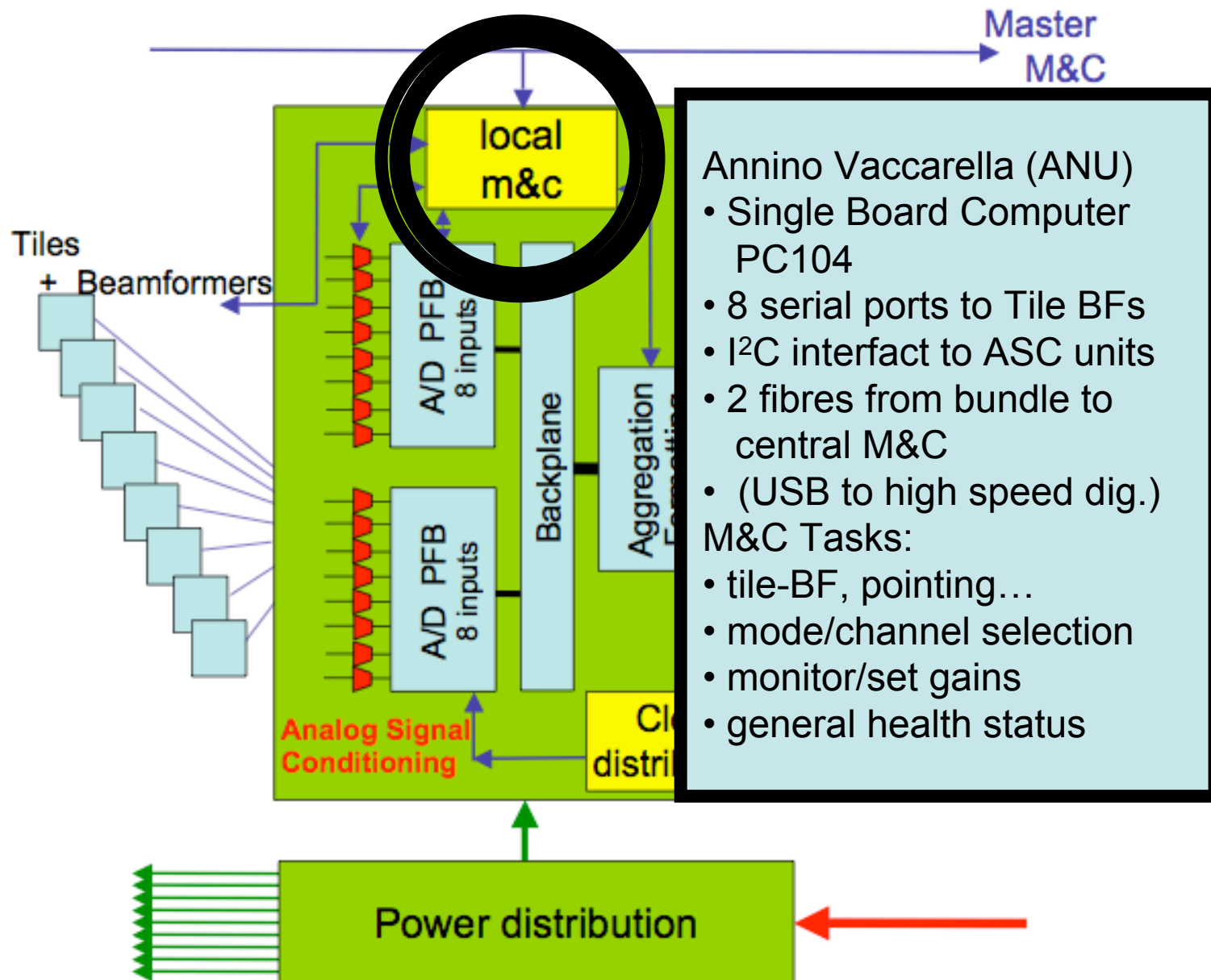
? Needs Specifications to  
Correlator/Transport Layer ?  
(ANU+, ATNF/CSIRO, Domain46)

- 500T... integrate into the  
A/D+PFB board



# 32T / Prototyping Layout !

## Receiver Node principal components



Annino Vaccarella (ANU)

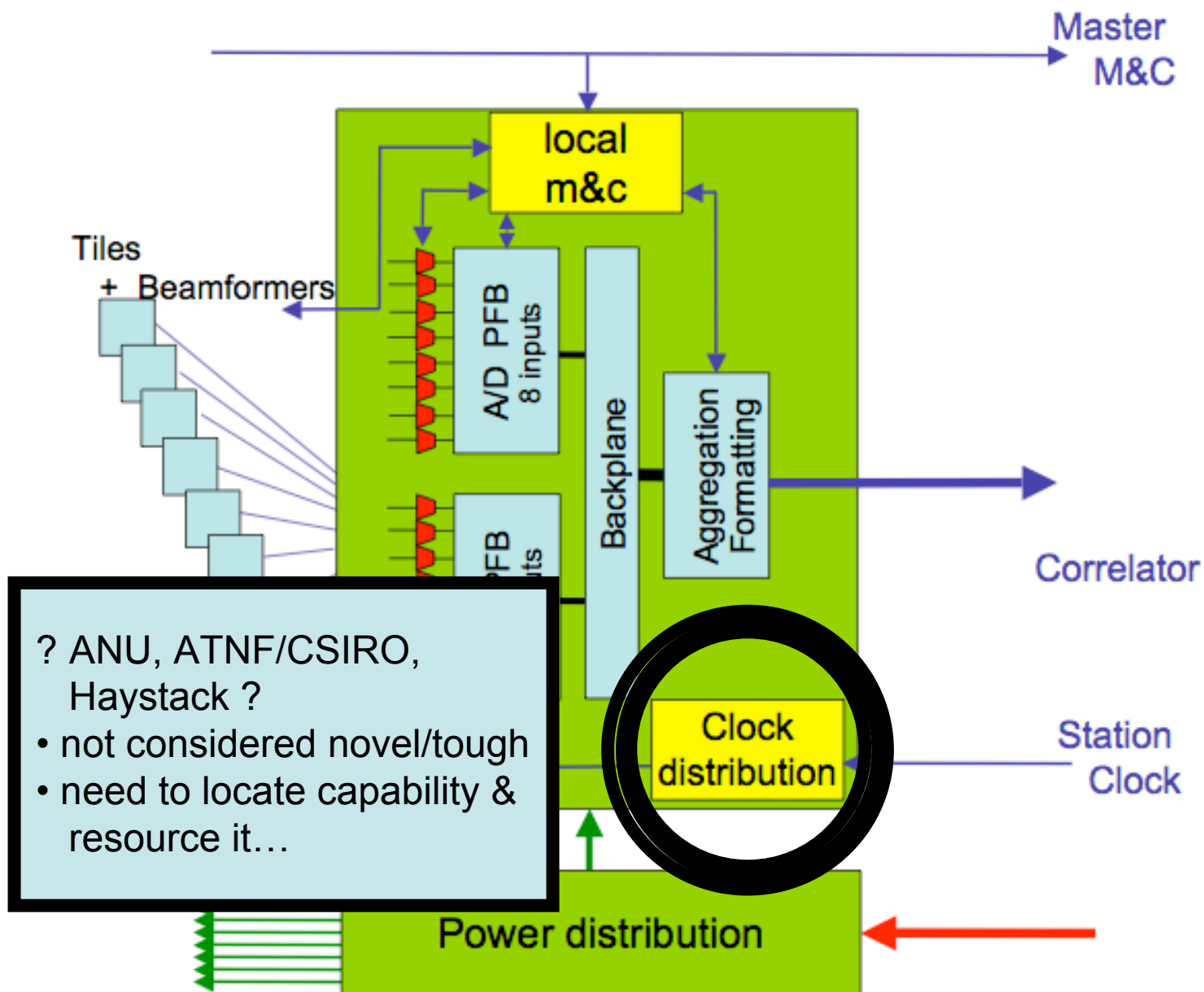
- Single Board Computer PC104
- 8 serial ports to Tile BFs
- I<sup>2</sup>C interfact to ASC units
- 2 fibres from bundle to central M&C
- (USB to high speed dig.)

M&C Tasks:

- tile-BF, pointing...
- mode/channel selection
- monitor/set gains
- general health status

# 32T / Prototyping Layout !

## Receiver Node principal components

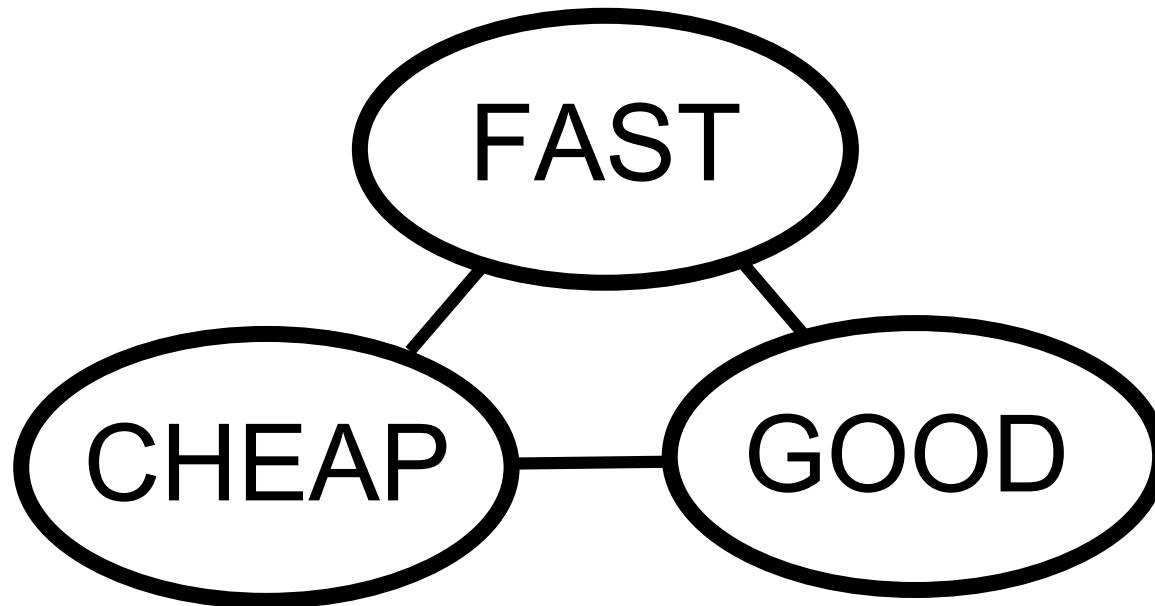


# Node & Receiver timeline

- modularizable...
- but, needs ~ FTE year
- ASCs, m&c ... OK
- ICT digital boards... firmware is lacking
- RSAA electronics pre-booked until mid-year

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Pick any 2 !

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- If must be fast, then needs more resource...
  
- or not-so-good...
  - ? Start with 8T, put “unpackaged” Node unit in caravan ?

# Node & Receiver cost uncertainty

- cost of FPGA chips... !  
9 x \$500 x 64 = \$0.3M