

MWA-LFD Correlator Architecture



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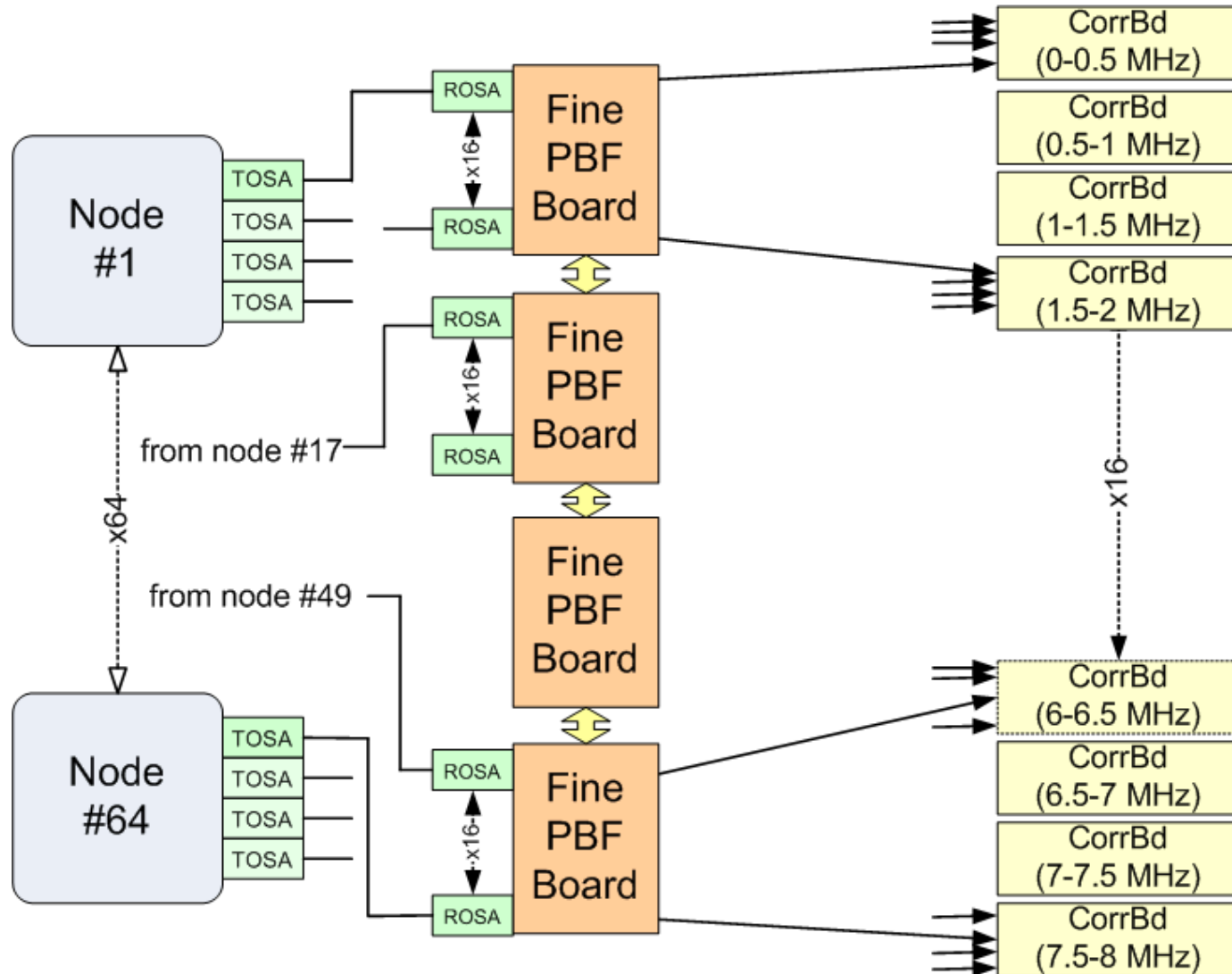


Big Decision: 32 or 28 MHz?

- 32 MHz achievable by:
 - Dropping PFB 8/7 oversampling factor
 - Channels near coarse band-edges vary in gain
 - Architecture more dissimilar from SKAMP
 - Buying significantly more hardware
 - 4 fibers + transmission + receiving logic per node (vs. 2)
 - 16 PFB boards in 2 ATCA shelves (vs. 8 in 1)
 - 64 correlator boards in 5 ATCA shelves (vs. 56 in 4)
 - Power for 25% more correlation (80 boards vs. 64)

Data Transport Layer

8 MHz slice - using 4 fibers per node





56 MHz option

- 2 fibers from each of 8 nodes go to 1 PFB
- 8 PFB boards in single card cage produce 28 MHz of “flat” bandwidth, with 3.5 MHz per PFB board
- 7 pairs of cables from each PFB carry data to 7 correlator boards
- Each correlator board processes 0.5 MHz of BW



Mapping Strategy of Correlation Pairs to Boards

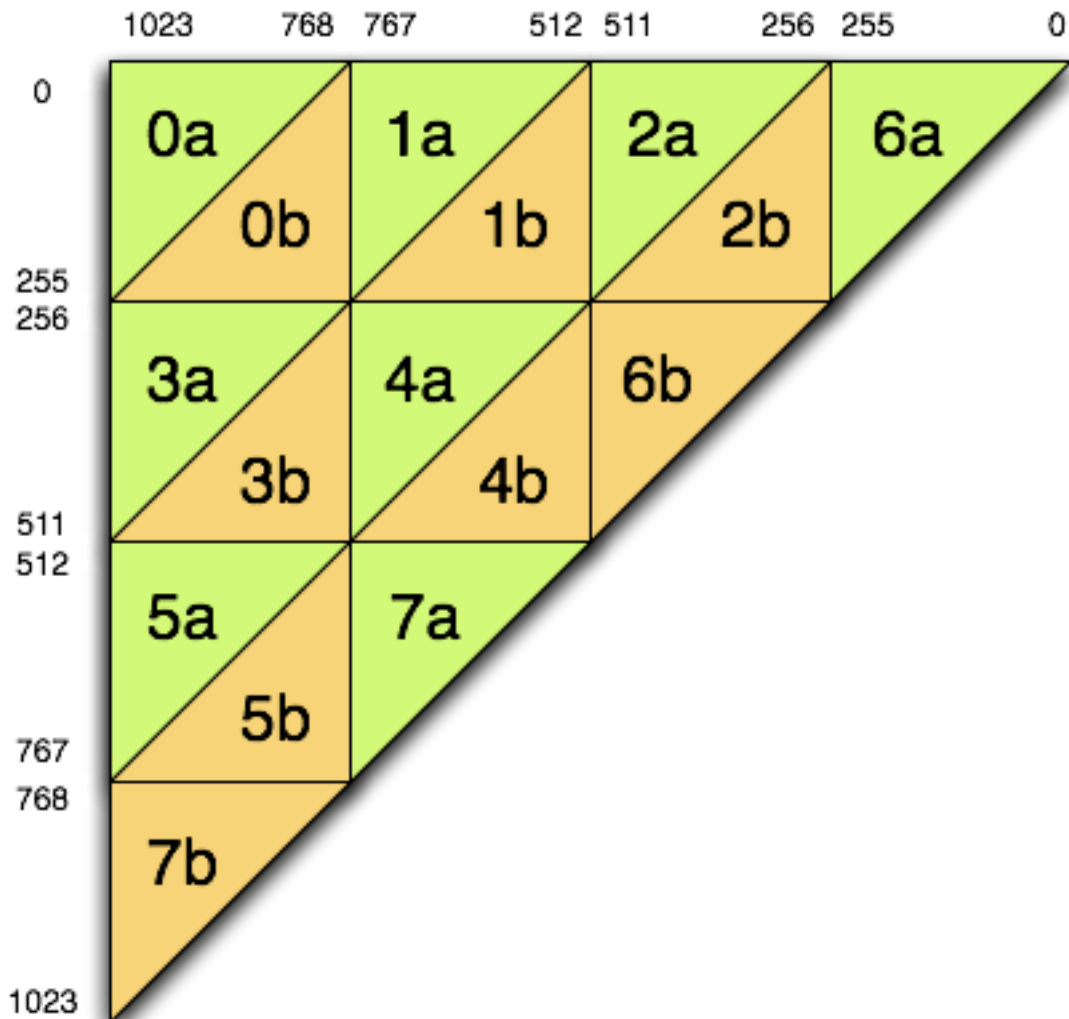
- Each board has 1536 DSP cells
- 16x16 antenna array per cell yields 393K pairs; practical # more like 250-300K
- Total pairs to do: 524K
- Two strategies to get all pairs
 - 1 pass: use 2 boards, each getting 1 MHz
 - 2 pass: use 1 board, each getting 0.5 MHz



1-pass vs. 2-pass: Tradeoffs

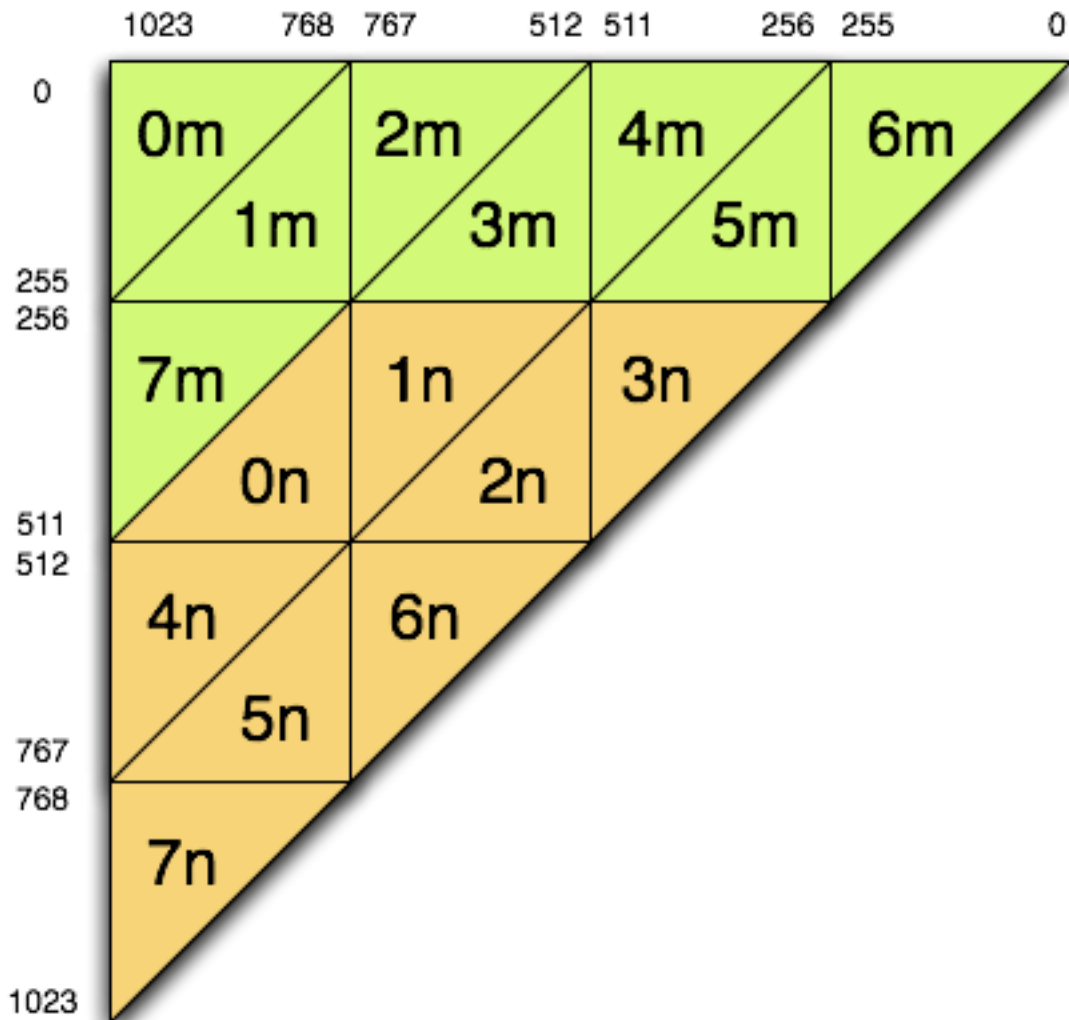
- In 1-pass all antennas for 1 MHz slice need to be sent to both boards, doubling the dataflow from PFB to correlator (16→32 Gb/s output per PFB board)
- 1-pass has simpler buffering on input to correlator board (all antennas for 1 time vs. 128 t's, or 256 t's with an FX-40)

Two-pass Correlation Layout



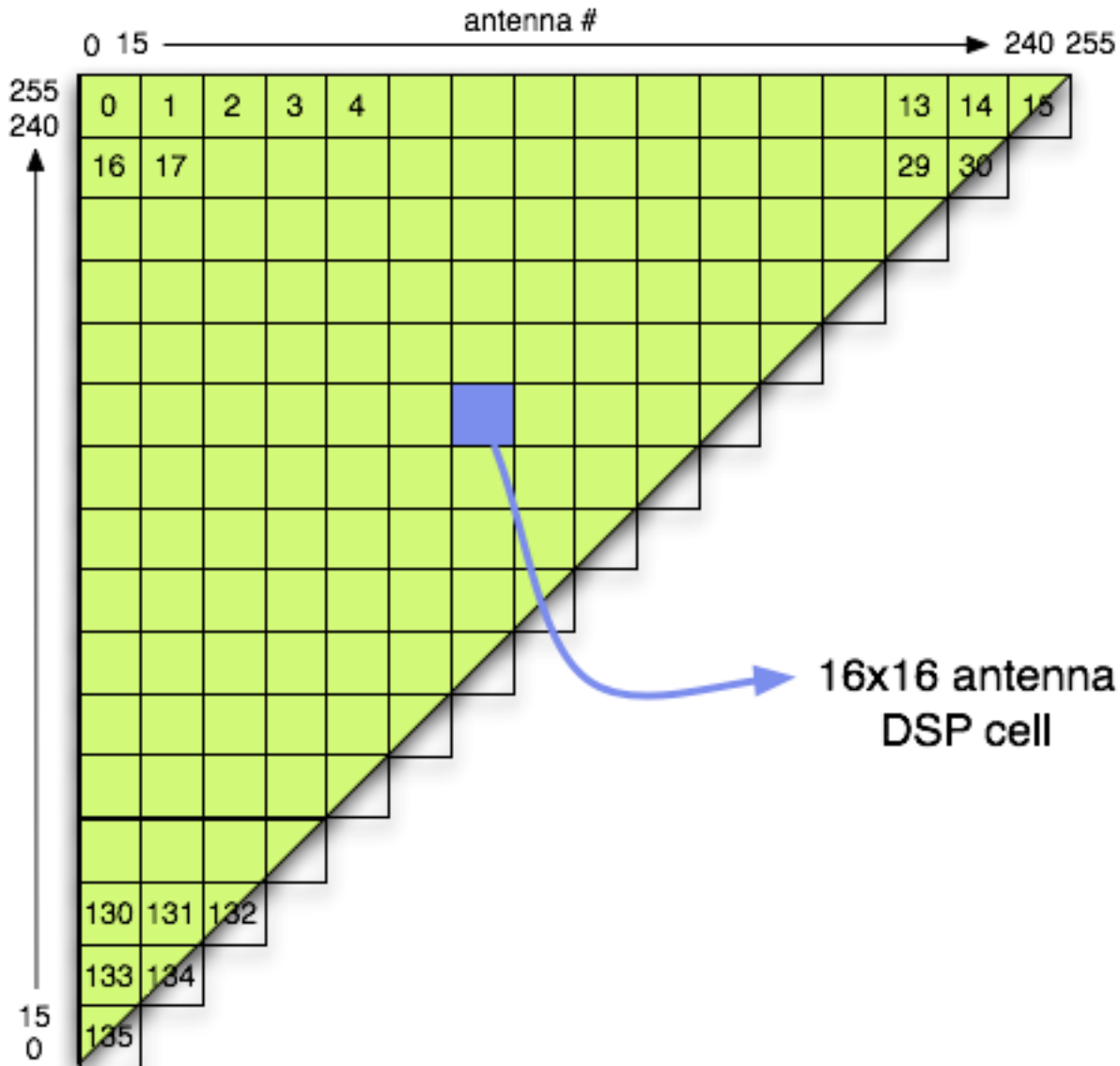
- Index 0..7 refers to SX-35 chip
- **a** and **b** are two consecutive passes
- On each pass, a triangular region of 256 x and 256 y antennas is processed

One-pass Correlation Layout



- Index 0..7 refers to SX-35 chip
- **m** and **n** are two adjacent correlator boards
- On each chip, a triangular region of 256 x and 256 y antennas is processed

DSP Cells within SX-35 Chip



- 136 of 192 DSP slices used
- Minor duplication of pairs along diagonal
- Lower diagonal half is done using opposite input order, with same routing in chip



Data Ordering - node to PFB

- Entering PFB board (2 fibers from each node) 2560 bit packets contain:
 - For each time ($0.875 \mu\text{s}$)
 - For each of 8 tile signals
 - 32 frequency samples (0.875 MHz; 5+5 bits; positive freqs. only)



Data Ordering - PFB to correlator board (2-pass)

- Entering correlator board (2 of 14 cables from a PFB) data stream consists of:
 - For each of 64 fine freq. channels (7 KHz)
 - For each of 128 time points (spanning 14 ms)
 - Packets containing 1024 antenna bytes (8K bits total; 4+4 bit complex)



Data Ordering - correlator routing chip to CMAC (2-pass)

- Entering CMAC chip on correlator board data stream consists of:
 - For each of 64 fine freq. channels (7 KHz)
 - For each of 2 correlator passes
 - For each of 128 time points (spanning 14 ms)
 - 256 x bytes and 256 y bytes (per us)